16-Channel Discriminator/Scaler VME Module
Revision C

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Overview

The 16-Channel Discriminator/Scaler Board contains 16 non-updating dual-threshold discriminators, programmable digital delays, and two 32-bit scalers per discriminator and threshold. The discriminator pulses are output as differential ECL logic levels through two front-panel headers. One group of outputs will connect to a TDC and the other group can be used as input to trigger logic. Both TDC and trigger output channels can individually be enabled/disabled with outputs widths and delays being user programmable. All programming is done through VME registers.

All discriminators and logic reside on a 6U VME64x mainboard. Each channel contains two analog receiver fast comparators (discriminator), and pulsers. Each discriminator channel has 2 programmable thresholds which can be programmed from VME. The output pulse width is also programmable from VME, but is common to the TDC and trigger discriminator channels separately. The TDC output is driven from the discriminator channel and not routed through the FPGA to minimize jitter and delays. The trigger (TRG) output is the second threshold per discriminator and is routed through the FPGA. The TRG output can be delayed in 4ns steps up to 512ns and the pulse reshaped in the FPGA to provide a 4 to 64ns pulse width. A TRG output delay setting of zero bypasses delay and pulse reshaping logic.

Each discriminator output pulse is recorded by two 32 bit counters (scaler). For each channel an external gate (NIM) is applied to one scaler while the other scaler is free running. Scalers can be latched, read, and cleared through VME. There is a "OR" (NIM level) ouput that is the logical OR of all the unmasked discriminator outputs.

Discriminator outputs are provided as dECL levels on the front panel for interfacing with TDCs and trigger logic.
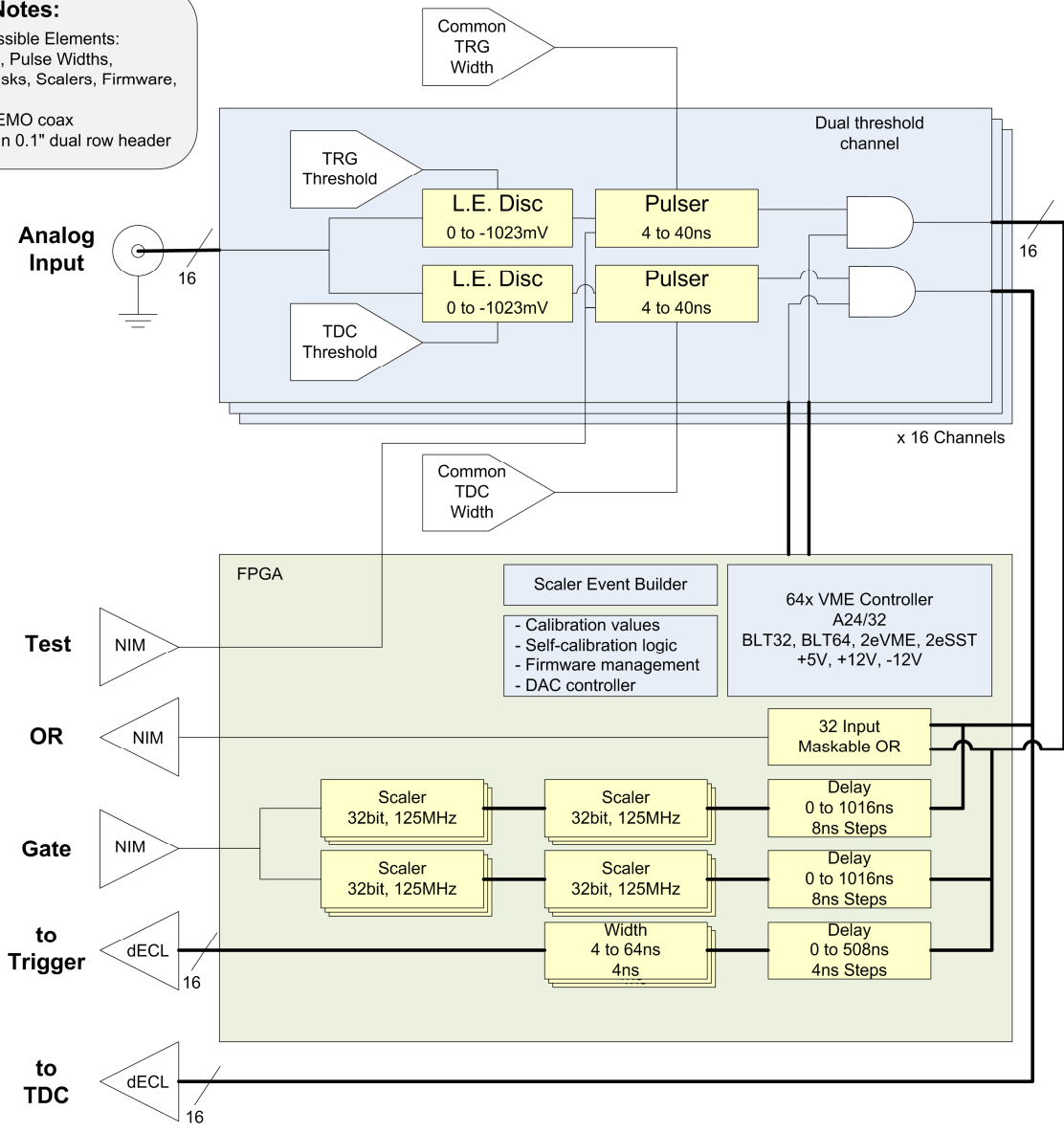
The VME64x interface is A32/A24/D32/D64/BLT32/BLT64/2eVME/2eSST with support for interrupts.

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Discriminator/Scaler Block Diagram

General Notes:
1) VME Accessible Elements:
   Thresholds, Pulse Widths,
   Delays, Masks, Scalers, Firmware,
   Calibration
2) NIM I/O: LEMO coax
3) dECL: 34pin 0.1" dual row header

Common TRG Width

Dual threshold channel

TRG Threshold

Analog Input

L.E. Disc
0 to -1023mV

Pulser
4 to 40ns

L.E. Disc
0 to -1023mV

Pulser
4 to 40ns

TDC Threshold

16

16

x 16 Channels

Common TDC Width

FPGA

Scaler Event Builder

64x VME Controller
A24/32
BLT32, BLT64, 2eVME, 2eSST
+5V, +12V, -12V

Test — NIM

- Calibration values
- Self-calibration logic
- Firmware management
- DAC controller

OR — NIM

32 Input
Maskable OR

Gate — NIM

Scaler
32bit, 125MHz

Scaler
32bit, 125MHz

Delay
0 to 1016ns
8ns Steps

Scaler
32bit, 125MHz

Scaler
32bit, 125MHz

Delay
0 to 1016ns
8ns Steps

to Trigger — dECL

Width
4 to 64ns
4ns

Delay
0 to 508ns
4ns Steps

16

to TDC — dECL

16

Specifications

General	Spec
Power consumption	+/-12v, 500mA; +5v, 5.0A (30W typ.)
Fuses	+/-12v, 1.0A; +5v, 10.0A
Dimensions	6U VME, Single-wide; 160mm card depth
Front Panel I/O	Input Signals: 16 LEMO
	Gate Input: 1 LEMO
	Test Input: 1 LEMO
	Dual dECL Output: 2x34 Header
	OR Output: 1 LEMO
Onboard connectors	JTAG: 2x7pin 2mm Xilinx
LEDs	Green: VME Activity/Power
	Yellow: TDC Discriminator OR
	Red: TRG Discriminator OR

Analog Inputs	From PMT or coaxial detector signals
Channels	16
Signal Level	+/-1.5v, DC-coupled, clamped
Termination	50ohm

Gate Input	Gates scalers (NIM, 50ohm termination jumper selectable)
Test Input	Pulses Discriminator Outputs (NIM, 50ohm termination jumper selectable)
OR Output	1 (NIM)

Discriminator Channels	
Dual threshold control	0 to -1023mV Threshold
	(for each TDC and TRG output)
Pulser	Non-updating
Pulser Width control	4ns to 40ns width +/-1ns accuracy
Pulser dead-time	~4ns w/8ns Pulse Width, ~10ns w/40ns Pulse Width
Maximum rate	80MHz w/8ns pulse setting
Channel-Channel Crosstalk	>65dB Isolation
Input Hysteresis	~5mV
Input Noise band	<2mV RMS, 1.3mV RMS typ.
Offset Error	<3mV max, <1mV typ.

dECL Outputs	
Channels	Dual 16 channel output
Connector	34pin header in LeCroy ECL format
1st group of 16 (TDC output)	Fast discriminator output
	Common width: 4 to 40ns
	Programmable mask register
2nd group of 16 (TRG output)	Common width 4 to 60ns
	Programmable mask register
Channel Threshold Control	10bit 1mV step (0 to -1023mV, +2048mV to -2047mV with firmware update)

Digital Delays	Trigger Out	Scaler/Gate
Delay step size	4ns	8ns
Delay range	0 to 508ns	0 to 1016ns
Uncertainty	4ns	8ns
Input/Gate timing alignment	Matched	

Scalers

Quantity   2 per threshold: 1 gated 1 free running
Width   32bit
Input source   Digital delay
Gating   External & free run scalers
Maximum Count rate   125MHz
Readout dead-time   None
Control   VME latch, read, clear, overflow, event build

VME Interface
Protocols   A32/A24,D32/D64/BLT32/BLT64/2eVME/2eSST
Address space   64kbyte

Misc
EEPROM   2Mbyte
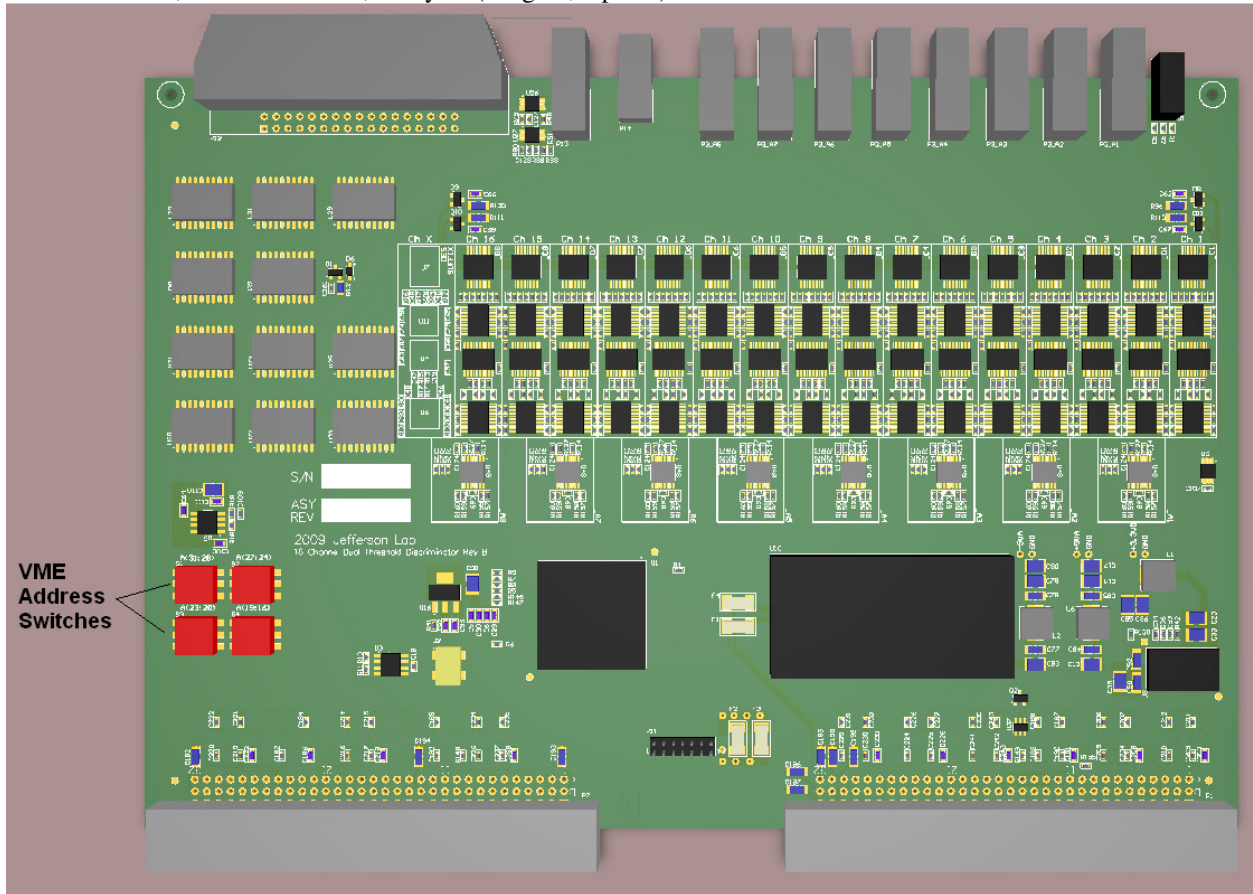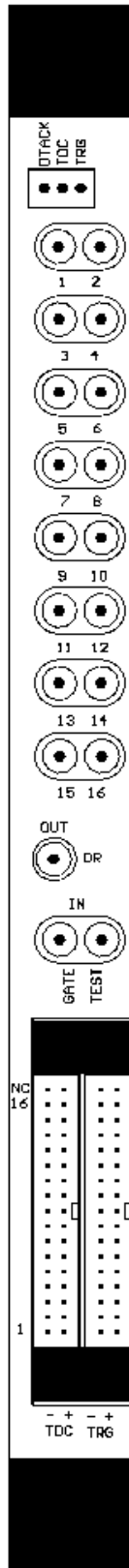Firmware Upgradable   Using VME

Delays
Input -> TDC Output   <6ns, <4.5ns typ.
Input-> TRG Output   15ns typ.

PCB Overview

FR406 substrate, 1/16" Thickness, 8 Layers (4 signal, 4 plane)

Front Panel

dECL Output Connector J1
(To TDC)

Pin	Function	Pin	Function
1	Ch 1 +	2	Ch 1 -
3	Ch 2 +	4	Ch 2 -
5	Ch 3 +	6	Ch 3 -
7	Ch 4 +	80	Ch 4 -
9	Ch 5 +	10	Ch 5 -
11	Ch 6 +	12	Ch 6 -
13	Ch 7 +	14	Ch 7 -
15	Ch 8 +	16	Ch 8 -
17	Ch 9 +	18	Ch 9 -
19	Ch 10 +	20	Ch 10 -
21	Ch 11 +	22	Ch 11 -
23	Ch 12 +	24	Ch 12 -
25	Ch 13 +	26	Ch 13 -
27	Ch 14 +	28	Ch 14 -
29	Ch 15 +	30	Ch 15 -
31	Ch 16 +	32	Ch 16 -
33	No Connect	34	No Connect

dECL Output Connector J2
(To Trigger Input)

Pin	Function	Pin	Function
1	Ch 1 +	2	Ch 1 -
3	Ch 2 +	4	Ch 2 -
5	Ch 3 +	6	Ch 3 -
7	Ch 4 +	80	Ch 4 -
9	Ch 5 +	10	Ch 5 -
11	Ch 6 +	12	Ch 6 -
13	Ch 7 +	14	Ch 7 -
15	Ch 8 +	16	Ch 8 -
17	Ch 9 +	18	Ch 9 -
19	Ch 10 +	20	Ch 10 -
21	Ch 11 +	22	Ch 11 -
23	Ch 12 +	24	Ch 12 -
25	Ch 13 +	26	Ch 13 -
27	Ch 14 +	28	Ch 14 -
29	Ch 15 +	30	Ch 15 -
31	Ch 16 +	32	Ch 16 -
33	No Connect	34	No Connect

VME Accessible Registers

All discriminator board registers can be accessed through the VME bus in the following modes:
- A24: single cycle accesses
- 32bit aligned read or write access (register specific)

Event readout can be access through the VME bus in the following modes:
- A32: single cycle, BLT, MBLT, 2eVME, 2eSST
- Note: transfer rate for 2eSST is 200MB/s

Register Summary:

Register	Description:	Address Offset-Range:
A_THRESHOLD_CH0	Threshold Control Ch0	0x0000
…	Threshold Control ChX	…
A_THRESHOLD_CH15	Threshold Control Ch15	0x003C
A_PULSEWIDTH	Pulse Width Control	0x0080
A_CH_ENABLE	Channel Control	0x0088
A_OR_MASK	OR Output Control	0x008C
A_DELAY	Input/Output Delays	0x0090
A_TEST	Test Input Control	0x0094
A_VME_LATCH	VME Scaler Latch	0x0098
A_LATCH	Gated Scaler Latch	0x009C
A_TRG_SCALER_CH0	Ext. Gate Trigger Scaler Ch0	0x0100
…	Ext. Gate Trigger Scaler ChX	…
A_TRG_SCALER_CH15	Ext. Gate Trigger Scaler Ch15	0x013C
A_TDC_SCALER_CH0	Ext. Gate TDC Scaler Ch0	0x0140
…	Ext. Gate TDC Scaler ChX	…
A_TDC_SCALER_CH15	Ext. Gate TDC Scaler Ch15	0x017C
A_TRG_VME_SCALER_CH0	VME Gate Trigger Scaler Ch0	0x0180
…	VME Gate Trigger Scaler ChX	…
A_TRG_VME_SCALER_CH15	VME Gate Trigger Scaler Ch15	0x01BC
A_TDC_VME_SCALER_CH0	VME Gate TDC Scaler Ch0	0x01C0
…	VME Gate TDC Scaler ChX	…
A_TDC_VME_SCALER_CH15	VME Gate TDC Scaler Ch15	0x01FC
A_REF_SCALER	VME Gate Ref Scaler	0x0200
A_REF_SCALER_GATE	Ext. Gate Ref Scaler	0x0204
A_FIRMWARE_REV	Firmware Revision	0x0400
A_BOARDID	Board Identifier	0x0404
A_READOUT_CLEAR	Clear Event Builder FIFO	0x0500
A_READOUT_START	Trigger Event Builder	0x504
A_MEM_ARRAY	Embedded CPU Shared Memory	0x8000-0x87FF
A_MEM_EXECUTE	Notify Embedded CPU	0x9000

Register: A_THREHOLD_CH0 -> A_THRESHOLD_CH15

Address Offset: 0x0000, 0x0004, …0x003C
Size: 32bits
Reset State: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	TRG Threshold	
23	22	21	20	19	18	17	16
TRG Threshold							
15	14	13	12	11	10	9	8
-	-	-	-	-	-	TDC Threshold	
7	6	5	4	3	2	1	0
TDC Threshold							

TDC Threshold (R/W):
    TDC CHx Threshold (in -1mV units)

TRG Threshold (R/W):
    TRG CHx Threshold (in -1mV units)

Notes:
1) TRG threshold should be >25mV above TDC threshold (for same channel) to avoid introducing jitter onto timing sensitive TDC comparator. If same thresholds are desired a firmware change can be made to route the TDC comparator output to TRG outputs.

Register: A_PULSEWIDTH

Address Offset: 0x0080
Size: 32bits
Reset State: 0xF03F003F

31	30	29	28	27	26	25	24
TRG Output Pulse Width				-	-	-	-
23	22	21	20	19	18	17	16
-	-	TRG Pulser Width					
15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-
7	6	5	4	3	2	1	0
-	-	TDC Pulser Width					

TDC Pulser Width (R/W):
    Controls pulser width (in units ns) for all TDC channels. Will be calibrated from 4ns to 40ns (~1ns accuracy). Values outside this range are not guaranteed to be calibrated.

TRG Pulser Width (R/W):
    Controls pulser width (in units ns) for all TRG channels. Will be calibrated from 4ns to 40ns (~1ns accuracy). Values outside this range are not guaranteed to work.

TRG Output Pulse Width (R/W):
    Digitally delayed/pulse trigger output pulse width: width = (TRGOutputPulseWidth+1)*4ns

Notes:
1) When TRG output delay (see corresponding register) is set to 0, the native TRG pulser width will appear on the TRG output as opposed to the digitally shaped pulse set be "TRG Output Pulse Width"

Register: A_CH_ENABLE

     Address Offset: 0x0088
     Size: 32bits
     Reset State: 0xFFFFFFFF

31	30	29	28	27	26	25	24
TRG15EN	TRG14EN	TRG13EN	TRG12EN	TRG11EN	TRG10EN	TRG9EN	TRG8EN
23	22	21	20	19	18	17	16
TRG7EN	TRG6EN	TRG5EN	TRG4EN	TRG3EN	TRG2EN	TRG1EN	TRG0EN
15	14	13	12	11	10	9	8
TDC15EN	TDC14EN	TDC13EN	TDC12EN	TDC11EN	TDC10EN	TDC9EN	TDC8EN
7	6	5	4	3	2	1	0
TDC7EN	TDC6EN	TDC5EN	TDC4EN	TDC3EN	TDC2EN	TDC1EN	TDC0EN

TDCENx (R/W):
     TDC Channel X: 1 = Enable, 0 = Disable

TRGENx (R/W):
     Trigger Channel X: 1 = Enable, 0 = Disable

Register: A_OR_MASK

     Address Offset: 0x008C
     Size: 32bits
     Reset State: 0x0000FFFF

31	30	29	28	27	26	25	24
TRG15EN	TRG14EN	TRG13EN	TRG12EN	TRG11EN	TRG10EN	TRG9EN	TRG8EN
23	22	21	20	19	18	17	16
TRG7EN	TRG6EN	TRG5EN	TRG4EN	TRG3EN	TRG2EN	TRG1EN	TRG0EN
15	14	13	12	11	10	9	8
TDC15EN	TDC14EN	TDC13EN	TDC12EN	TDC11EN	TDC10EN	TDC9EN	TDC8EN
7	6	5	4	3	2	1	0
TDC7EN	TDC6EN	TDC5EN	TDC4EN	TDC3EN	TDC2EN	TDC1EN	TDC0EN

TDCxEN (R/W):
     TDC Channel X: 1 = Enable in front-panel OR output, 0 = Not used in OR

TRGENx (R/W):
     Trigger Channel X: 1 = Enable in front-panel OR output, 0 = Not used in OR

Notes:
1) All TDC channels enabled in the above MASK are used to display the TDC front-panel LED
2) All TRG channels enabled in the above MASK are used to display the TRG front-panel LED

Register: A_DELAY

Address Offset: 0x0090
Size: 32bits
Reset State: 0x00080008

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	TRGOutputDelay						

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	ScalerDelay						

ScalerDelay (R/W):
Scaler Input Delay 0-127 count (in 8ns ticks)

TRGOutputDelay (R/W):
Trigger Output Delay 0-127 count (in 4ns ticks)

Notes:
1) See note in register A_PULSEWIDTH. When TRGOutputDelay = 0, the digital delay and pulse reshaping is bypassed providing a minimal delay output from the trigger channels using the TRG pulser width setting.

Register: A_TEST

Address Offset: 0x0094
Size: 32bits
Reset State: 0x00000001

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	TestEnable

TestEnable (R/W):
'0' – disables front-panel test input to discriminator channels
'1' – enables front-panel test input to discriminator channels

Notes:
1) When writing this register a software test pulse is sent to the discriminator channels (useful for testing channels by writing any value to this register).
2) When TestEnable register bit is enabled, a NIM logic level '1' must be supplied to front-panel test input signal to test fire the discriminator channels.

Register: A_VME_LATCH

      Address Offset: 0x0098

      Size: 32bits

      Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
VME_SCALER_LATCH							
23	22	21	20	19	18	17	16
VME_SCALER_LATCH							
15	14	13	12	11	10	9	8
VME_SCALER_LATCH							
7	6	5	4	3	2	1	0
VME_SCALER_LATCH							

      VME_SCALER_LATCH(WO):

            Write any value to latch VME scalers.

      Notes:

          1)   After latching scalers for readout, hardware scalers will be reset.

Register: A_LATCH

      Address Offset: 0x009C

      Size: 32bits

      Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
GATED_SCALER_LATCH							
23	22	21	20	19	18	17	16
GATED_SCALER_LATCH							
15	14	13	12	11	10	9	8
GATED_SCALER_LATCH							
7	6	5	4	3	2	1	0
GATED_SCALER_LATCH							

      GATED_SCALER_LATCH(WO):

            Write any value to latch gated scalers.

      Notes:

          1)   After latching scalers for readout, hardware scalers will be reset.

Register: A_READOUT_CLEAR

Address Offset: 0x0500
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
			READOUT_CLEAR				

23	22	21	20	19	18	17	16
			READOUT_CLEAR				

15	14	13	12	11	10	9	8
			READOUT_CLEAR				

7	6	5	4	3	2	1	0
			READOUT_CLEAR				

READOUT_CLEAR (WO):
> Write any value to clear event building FIFO.

Register: A_READOUT_START

Address Offset: 0x0504
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
			BUILDER_FLAG				

BUILDER_FLAG (R/W):
> bit 7: '1' latch gated scalers for event build. '0' do nothing.
> bit 6: '1' latch ungated scalers for event build. '0' do nothing.
> bit 5: '1' write ungated reference scaler for event build. '0' do nothing.
> bit 4: '1' write gate reference scaler for event build. '0' do nothing.
> bit 3: '1' write TDC ungated scalers for event build. '0' do nothing.
> bit 2: '1' write TRG ungated scalers for event build. '0' do nothing.
> bit 1: '1' write TDC gated scalers for event build. '0' do nothing.
> bit 0: '1' write TRG gated scalers for event build. '0' do nothing.

Notes:
> 1) Writing the register causes the scaler event builder to execute and fill the readout FIFO with a scaler event as defined by the BUILDER_FLAG field

Register: A_TRG_SCALER_CH0 -> A_ TRG_SCALER _CH15

Address Offset: 0x0100, 0x0104, …0x013C
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
			TRG SCALER				
23	22	21	20	19	18	17	16
			TRG SCALER				
15	14	13	12	11	10	9	8
			TRG SCALER				
7	6	5	4	3	2	1	0
			TRG SCALER				

TRG SCALER(RO):
Latched trigger threshold scaler for CHx. 32bit value indicates an overflow when count is saturated (at 0xFFFFFFFF). Scaler is incremented on discriminator channel event and when external input gate = NIM logic 1.

Notes:
1) A scaler latch must be performed (by writing to register A_LATCH) to update these registers with current scaler counts

Register: A_TDC_SCALER_CH0 -> A_ TDC_SCALER _CH15

Address Offset: 0x0140, 0x0144, …0x017C
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
			TDC SCALER				
23	22	21	20	19	18	17	16
			TDC SCALER				
15	14	13	12	11	10	9	8
			TDC SCALER				
7	6	5	4	3	2	1	0
			TDC SCALER				

TDC SCALER(RO):
Latched TDC threshold scaler for CHx. 32bit value indicates an overflow when count is saturated (at 0xFFFFFFFF) . Scaler is incremented on discriminator channel event and when external input gate = NIM logic 1.

Notes:
1) A scaler latch must be performed (by writing to register A_LATCH) to update these registers with current scaler counts

Register: A_TRG_VME_SCALER_CH0 -> A_ TRG_ VME_SCALER _CH15

      Address Offset: 0x0180, 0x0184, …0x01BC
      Size: 32bits
      Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
TRG VME SCALER							
23	22	21	20	19	18	17	16
TRG VME SCALER							
15	14	13	12	11	10	9	8
TRG VME SCALER							
7	6	5	4	3	2	1	0
TRG VME SCALER							

TRG SCALER(RO):
      Latched trigger threshold scaler for CHx. 32bit value indicates an overflow when count is saturated (at 0xFFFFFFFF). Scaler is incremented on discriminator channel event.

Notes:
1) A scaler latch must be performed (by writing to register A_VME_LATCH) to update these registers with current scaler counts

Register: A_TDC_VME_SCALER_CH0 -> A_ TDC_VME_SCALER _CH15

      Address Offset: 0x01C0, 0x01C4, …0x01FC
      Size: 32bits
      Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
TDC VME SCALER							
23	22	21	20	19	18	17	16
TDC VME SCALER							
15	14	13	12	11	10	9	8
TDC VME SCALER							
7	6	5	4	3	2	1	0
TDC VME SCALER							

TDC SCALER(RO):
      Latched TDC threshold scaler for CHx. 32bit value indicates an overflow when count is saturated (at 0xFFFFFFFF) . Scaler is incremented on discriminator channel event.

Notes:
1) A scaler latch must be performed (by writing to register A_VME_LATCH) to update these registers with current scaler counts

Register: A_REF_SCALER

Address Offset: 0x0200
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
REF VME SCALER							

23	22	21	20	19	18	17	16
REF VME SCALER							

15	14	13	12	11	10	9	8
REF VME SCALER							

7	6	5	4	3	2	1	0
REF VME SCALER							

REF VME SCALER(RO):

Latched reference scaler for VME gated scalers. 32bit value indicates an overflow when count is saturated (at 0xFFFFFFFF). Scaler is incremented at board clock rate (125MHz) and provides an accurate measurement of elapsed time since last latch of VME gated scalers.

Notes:

1) A scaler latch must be performed (by writing to register A_VME_LATCH) to update these registers with current scaler counts

Register: A_REF_SCALER_GATE

Address Offset: 0x0204
Size: 32bits
Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
REF GATE SCALER							

23	22	21	20	19	18	17	16
REF GATE SCALER							

15	14	13	12	11	10	9	8
REF GATE SCALER							

7	6	5	4	3	2	1	0
REF GATE SCALER							

REF GATE SCALER(RO):

Latched reference scaler for external gated scalers. 32bit value indicates an overflow when count is saturated (at 0xFFFFFFFF). Scaler is incremented at board clock rate (125MHz) and provides an accurate measurement of elapsed time since last latch of externally gated scalers.

Notes:

1) A scaler latch must be performed (by writing to register A_LATCH) to update these registers with current scaler counts

Register: A_FIRMWARE_REV

    Address Offset: 0x0400
    Size: 32bits
    Reset State: 0xXXXXXXXX

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
FIRMWARE_REV_MAJOR							

7	6	5	4	3	2	1	0
FIRMWARE_REV_MINOR							

FIRMWARE_REV_MAJOR(RO):
    Major firmware revision
FIRMWARE_REV_MINOR(RO):
    Minor firmware revision

Register: A_BOARDID

    Address Offset: 0x0404
    Size: 32bits
    Reset State: 0x44534332

31	30	29	28	27	26	25	24
BOARD_ID							

23	22	21	20	19	18	17	16
BOARD_ID							

15	14	13	12	11	10	9	8
BOARD_ID							

7	6	5	4	3	2	1	0
BOARD_ID							

BOARD_ID(RO):
    0x44534332 = "DSC2" in ASCII

Register: A_MEM_ARRAY

Address Offset: 0x8000-0x87FF

Size: 32bits

Notes:

1) This memory is reserved for testing, calibration, and firmware upgrade use.

Register: A_MEM_EXECUTE

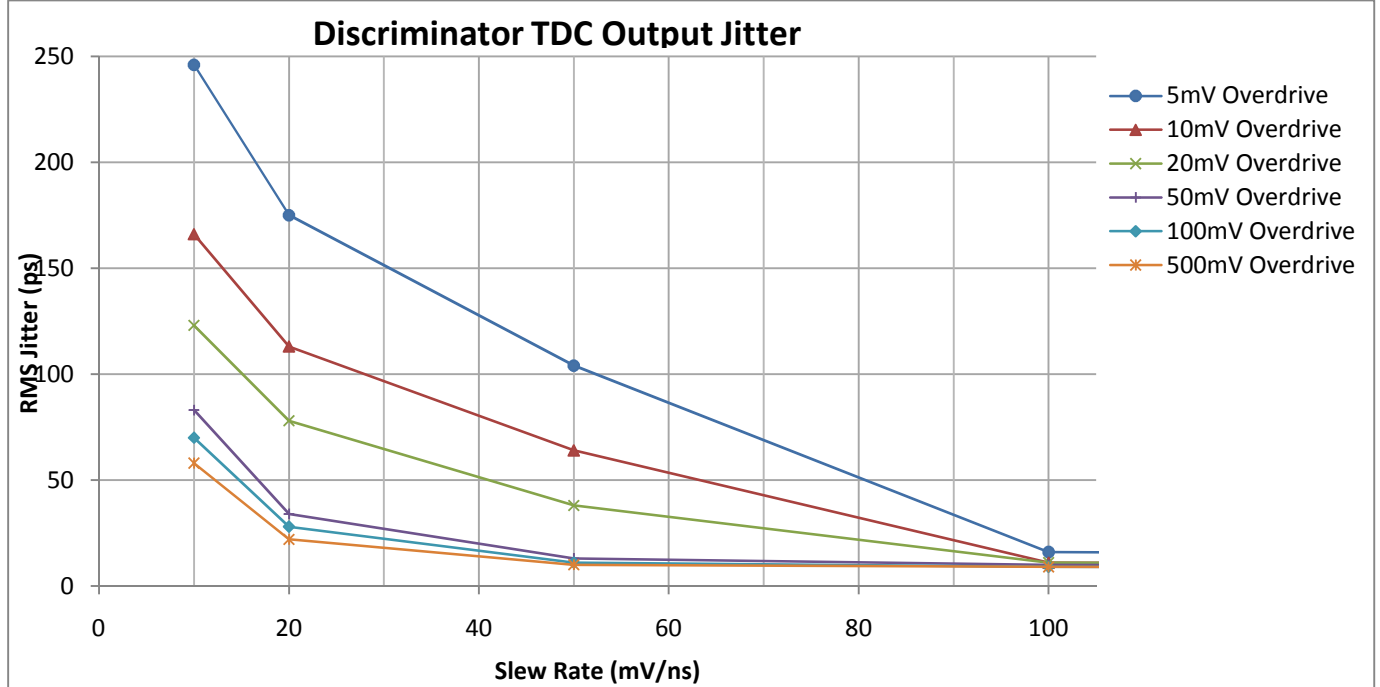Address Offset: 0x9000

Size: 32bits

Notes:

1) This register is reserved for testing, calibration, and firmware upgrade use.
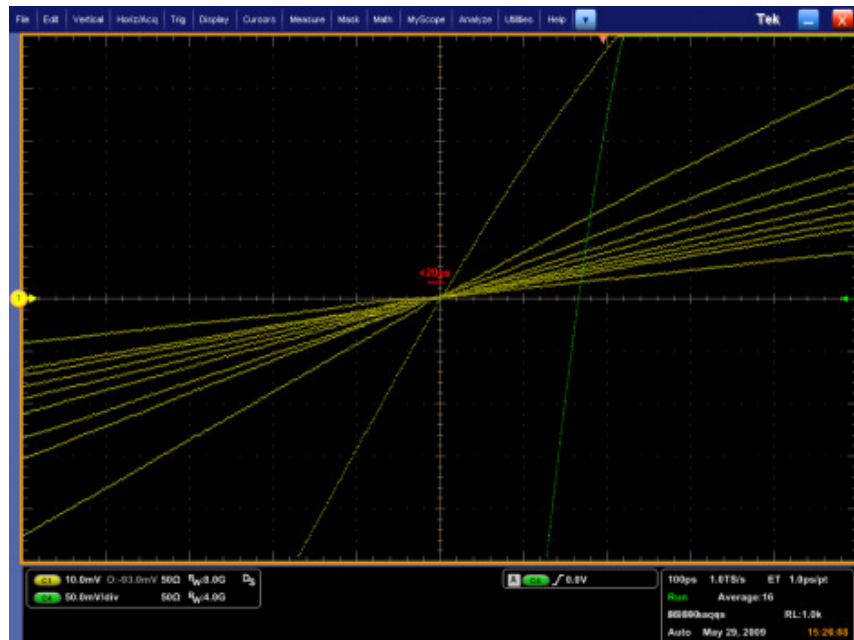
Module Performance (Typical)

Measured signal jitter:

      Input: 1Vpp, 1MHz square wave with an overdrive from 5mV to 500mV, and slew rate from 10mV/ns to 1000mV/ns. The following plot indicates measured performance.

Measured slew rate dispersion:

      356mV, 30ns width negative pulse. Overdrive set to 100mV, edge rate varied from 250mV/ns to 20mV/ns, pulse rate 100Hz. Roughly a 20ps dispersion with respect to slew rate measured.
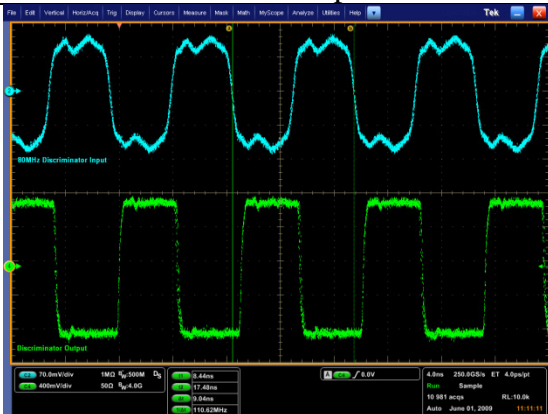
Measured channel isolation:

A 1V edge with slew rate 1V/ns injected into discriminator channel. The pickup measured on adjacent channels was less than 350µV (>69dB channel-channel isolation). Yellow trace below is measured induced voltage on victim channel.

Measured maximum rates:

110MHz Rate w/4ns Output Pulse Width	80MHz Rate w/8ns Output Pulse Width

FPGA Resource Usage

All features advertised in the manual have been implemented in current FPGA firmware. Resource usage is under 35% for general logic and under 60% for RAM. Plenty of expansion room remains for future needs. Firmware is remotely upgradeable through the VME interface and takes about 30 seconds per module to download and verify.

Device Utilization Summary (actual values)					[-]
Logic Utilization	Used	Available	Utilization	Note(s)	
Total Number Slice Registers	7,815	22,528	34%		
Number used as Flip Flops	7,814				
Number used as Latches	1				
Number of 4 input LUTs	8,091	22,528	35%		
Number of occupied Slices	6,939	11,264	61%		
Number of Slices containing only related logic	6,939	6,939	100%		
Number of Slices containing unrelated logic	0	6,939	0%		
Total Number of 4 input LUTs	10,390	22,528	46%		
Number used as logic	7,489				
Number used as a route-thru	2,299				
Number used for Dual Port RAMs	256				
Number used as Shift registers	346				
Number of bonded IOBs	243	375	64%		
IOB Flip Flops	205				
Number of BUFGMUXs	7	24	29%		
Number of DCMs	2	8	25%		
Number of ICAPs	1	1	100%		
Number of BSCANs	1	1	100%		
Number of BSCAN_SPARTAN3As	1	1	100%		
Number of ICAP_SPARTAN3As	1	1	100%		
Number of RAMB16BWEs	19	32	59%		
Number of RPM macros	13				
Average Fanout of Non-Clock Nets	3.16				

Scaler Event Readout

   Scaler event readout is performed by writing to the **A_READOUT_START** register with the appropriate flags set according to the user preference. Each time this register is written the internal event builder will write to the readout FIFO with the scaler event determined by the flags set. Events can be generated until the readout FIFO not longer contains enough space for a full event to be written. This guarantees that only full events are written and never partial events. If all flags are set, 7 events can be stored in the readout FIFO before any readout is performed. Readout is performed by accessing the modules A32 VME address using any of the support VME protocols of this board.

   The following outlines the scaler event readout format (each line represents a 32bit word):
- a)   <EVENT HEADER>
- b)   <TRG0 GATED SCALER>

  …
  <TRG15 GATED SCALER>
- c)   <TDC0 GATED SCALER>

  …
  <TDC15 GATED SCALER>
- d)   <TRG0 UNGATED SCALER>

  …
  <TRG15 UNGATED SCALER>
- e)   <TDC0 UNGATED SCALER>

  …
  <TDC15 UNGATED SCALER>
- f)   <GATED REFERECE SCALER>
- g)   <UNGATED REFERECE SCALER>

Section (a) <EVENT HEADER> format:
  bits 31:13   1101_1100_1010_0000_000
  bits 12:8 Geographic slot ID (is 11110 when parity error exists or in non 64x VME crate)
  bits 7:0   8bit flags defined in A_READOUT_START that triggered this event build
Section (b) <TRGx GATED SCALER>
  When A_READOUT_START->BUILDER_FLAG bit 0 is set, the 16 TRG GATED 32bit scaler values are put in the event for readout.
Section (c) <TDCx GATED SCALER>
  When A_READOUT_START->BUILDER_FLAG bit 1 is set, the 16 TRG GATED 32bit scaler values are put in the event for readout.
Section (d) <TRGx UNGATED SCALER>
  When A_READOUT_START->BUILDER_FLAG bit 2 is set, the 16 TRG UNGATED 32bit scaler values are put in the event for readout.
Section (e) <TDCx UNGATED SCALER>
  When A_READOUT_START->BUILDER_FLAG bit 3 is set, the 16 TRG UNGATED 32bit scaler values are put in the event for readout.
Section (f) <GATED REFERENCE SCALER>
  When A_READOUT_START->BUILDER_FLAG bit 4 is set, the GATED reference 32bit scaler value is put in the event for readout.
Section (g) <TDCx UNGATED SCALER>
  When A_READOUT_START->BUILDER_FLAG bit 5 is set, the UNGATED reference 32bit scaler value is put in the event for readout.

   Note: for 64bit VME protocols, additional filler words may follow to satisfy VME transaction word count requirements. This module will bus error at the completion of a single event readout – this is the recommended way to readout this module to ensure the full event has been read from this module.