A VME64x, 16-Channel, Pipelined 250 MSPS Flash ADC With Switched Serial (VXS) Extension

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Abstract - We have designed a 250 MSPS pipelined flash ADC (Analog-to-Digital Converter) which will be employed at the Jefferson Lab's four experimental physics halls. This high speed and high density flash ADC conforms to VITA-41 VME64x switched serial (VXS) standard.

I. Introduction

A high speed and high density flash ADC module has been designed for use in nuclear physics experiments at Jefferson Lab. The Continuous Electron Beam Accelerator at Jefferson Lab currently delivers 6 GeV electrons to three experimental end stations. As part of a planned energy upgrade to 12 GeV electrons, a new experimental end station (Hall D) will be built and instrumented. A high speed and pipelined flash ADC will be used to provide information about the energy deposited on a detector element or group, timing, hit and trigger information.

The trigger information output from each of the modules on a VXS crate is routed via the backplane to a switch slot. A total of 18 flash ADCs per crate feed serial data to the switch slot at an aggregate rate of 6 Gb/s which is then sent to the experiment global VXS trigger crate.

Figure 1 shows some of the components of a typical VXS crate to be used at Jefferson Lab[2]: fADCs, an energy sum output switch card, a switch card for clock and timing distribution and a backplane.

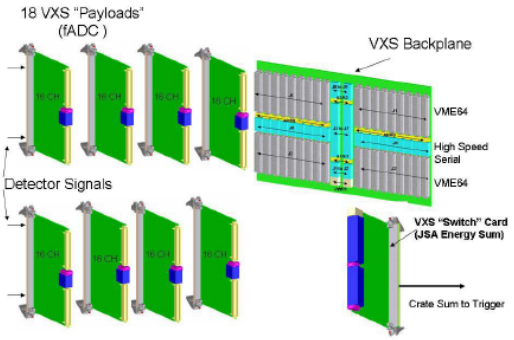

Figure 1: VXS Crate Components

II. The Flash ADC Module

The flash ADC module has been designed to accept 8-, 10- or 12-bit ADC chips. The choice of the chip will depend on the application resolution requirements and cost. The architecture of the fADC is shown in figure 2.

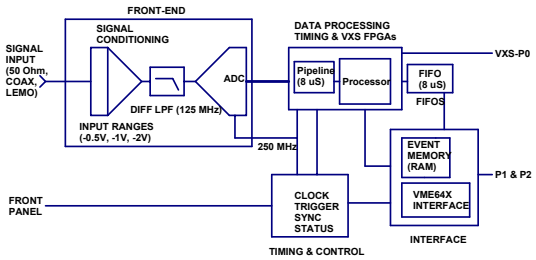

Figure2: Simplified fADC Architecture

There are three user-selectable ranges available for each of the inputs and differential signal conditioning scales the input signals to within the dynamic range of the ADCs. A single-pole low-pass filter limits the signal bandwidth to the Nyquist band of the converter or 125 MHz. Individual channel offsets are effected by means of DACs under VME control. For the 10-bit version of the flash ADC, the INL and DNL are expected to be ± 0.8 LSB and ± 0.5 LSB, respectively.

The digitized LVDS data and clock signals are then fed to a set of Virtex 4 LX25 FPGAs for data processing and temporary storage at the full 250 MSPS rate. ADC data is stored in RAM for event building and readout via VME. Additionally, these FPGAs output 16-bit energy sum words and channel hit information.

A Virtex 4 FX20 FPGA effects the board energy sum for output through the VXS connector via the RocketIO Multi-Gigabit Transceivers (MGT).

A fourth STRATIX II FPGA handles the control, trigger and interface functions. The VME 2eSST data transfer cycles can reach up to 320 MB/s.

The depth of the pipeline is 8 us and windowing and trigger latency are user programmable. In addition, sparcification, charge, pedestal and peak values may be

obtained, as well as, hit information with user-defined thresholds and trigger processing.

In order to take full advantage of this high speed ADC, a differential PECL clock with jitter specification of less than 2 ps is timed properly across the various clock domains.

III. Results

The fADC prototype board is shown in figure 3. This 14-layer high density board employs fine pitch components on both sides and takes advantage of impedance matched micro-strip lines. The FPGAs' packages are of the BGA type and the ADC chips use QFN packages for improved thermal performance.

Figure 3: The 250 MSPS fADC

The 250 MHz differential PECL clock is shown in Figure 4. Its jitter was measured to be less than 2 ps.

Figure 4: The 250 MHz Sampling Clock

The front end signal response to a 10 ns wide pulse is shown in figure 5. The pulses at the top of the picture are the differential inputs to the ADC chip after being conditioned and filtered by the input low pass filter; the pulse at the bottom is the difference of the above signals and represents what the ADC chip actually digitizes. The front end bandwidth was measured to be 110 MHz.

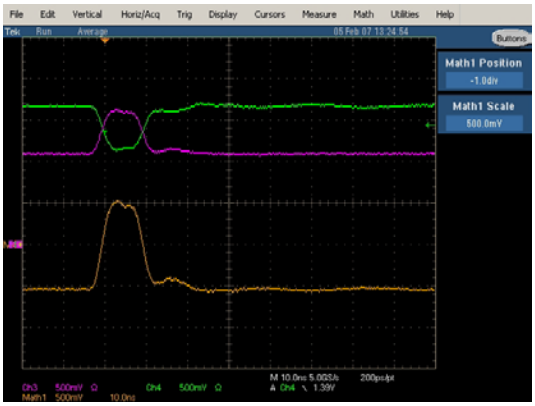

Figure 5: Front End Pulse Response

IV. Conclusion

We have designed and assembled a high density 250 MSPS flash ADC for use in physics experiments. This prototype, which is currently undergoing tests, will be used to further study the data transfer characteristics of the VXS standard conforming to VITA-41 and to implement algorithms in the study of detector signals for energy deposition, timing and triggering in realistic conditions expected in the experimental end stations at Jefferson Lab.

V. References

[1] H. Dong, C. Cuevas, D. Curry, E. Jastrzembski, F. Barbosa, J. Wilson, M. Taylor, " VXS Switch Card for High Density Data Acquisition System", IEEE SoutheastCon 2007, Richmond, VA, March 22-25, 2007.

VI. Acknowledgements

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